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APPLICATION NO. 10/009826

August 3, 2004

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CLMPTO

1. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit disposed on the semiconductor substrate;

wherein ~~the~~ each memory cell has a multi-layer of a conductive layer, an insulating layer and plural semiconductor layers containing impurities of different conduction type, and

a potential ~~can be~~ applied to the insulating layer ~~that~~ enables ~~the~~ movement of carriers ~~by way of~~ through the multi-layer, and

at least said plural semiconductor layers are disposed below a surface of said semiconductor substrate.

2. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit disposed on the semiconductor substrate;

wherein ~~the~~ each memory cell has a multi-layer of a conductive layer, an insulating layer and plural semiconductor layers containing impurities, and

the multi-layer of the each memory cell has bistable characteristics for the a resistance value,

a potential applied to the insulating layer enables movement of carriers through the multi-layer, and

at least said plural semiconductor layers are disposed below a surface of said semiconductor substrate.

3. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit, disposed on the semiconductor substrate, ~~which is constituted with~~ having plural insulated gate field effect transistors (MISFET) on the a periphery of the memory cell array;

wherein ~~the~~ each memory cell has a multi-layer of a conductive layer, an insulating layer that enables ~~the~~ a tunneling effect, and plural semiconductor layers containing impurities, and

the plural semiconductor layers ~~containing impurities~~ are present in the semiconductor substrate, and

at least said plural semiconductor layers are disposed below a surface of said semiconductor substrate.

4. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein the plural semiconductor layers containing impurities ~~constituting the memory cell~~ have two semiconductor layers of different p-type and n-type conduction.

5. (Currently Amended) A semiconductor memory device as defined in claim 4, wherein a position of a junction formed ~~of~~ by the two semiconductor layers of different p-type and n-type conduction ~~of the memory cell~~ is shallower than the depth of a device isolation region formed in the semiconductor substrate.

6. (Currently Amended) A semiconductor memory device as defined in claim 4, wherein a position of a PN junction of ~~the~~ each memory cell is shallower than the depth of 0.3 μm from the surface of the semiconductor substrate.

7. (Currently Amended) A semiconductor memory device as defined in claim 4, wherein at least one of the plural semiconductor layers ~~containing impurities of the memory cell~~ has a an impurity concentration that is higher ~~in the~~ inside of the semiconductor substrate than on the surface of the semiconductor substrate.

8. (Currently Amended), A semiconductor memory device as defined in claim 4, wherein an impurity concentration of the a layer present in contact with the surface of the

semiconductor substrate ~~among~~ of the plural semiconductor layers ~~containing impurities for forming the memory cell~~ is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.

9. (Currently Amended) A semiconductor memory device as defined in claim 4, wherein a maximum impurity concentration of a layer ~~present~~ in contact with the surface of the semiconductor substrate ~~among~~ of the plural semiconductor layers ~~containing impurities for forming the memory cell~~ is 1×10^{17} cm^{-3} or more.

10. (Currently Amended) A semiconductor memory device as defined in claim 4, wherein a maximum impurity concentration of ~~the~~ a layer present ~~in the~~ inside of the semiconductor substrate ~~among~~ of the plural semiconductor layers ~~containing impurities for forming the memory cell~~ is 1×10^{17} cm^{3} or more.

11. (Currently Amended) A semiconductor memory device as defined claim 4, wherein a position of a PN junction of ~~the~~ each memory cell is at a place deeper than a position at which an impurity concentration is

maximum of a layer present in contact with the surface of the semiconductor substrate ~~among~~ of the plural semiconductor layers ~~containing impurities for forming the memory cell~~.

12. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein the plural semiconductor layers ~~containing impurities of the memory cell~~ comprise two ~~P-type~~ p-type layers ~~putting~~ with an ~~N-type~~ n-type layer therebetween, or two ~~N-type~~ n-type layers ~~putting~~ with a ~~P-type~~ p-type layer therebetween.

13. (Currently Amended) A semiconductor memory device according to claim 5 wherein ~~which two P-type layers and an N-type layer precent apart from the surface semiconductor substrate among the three semiconductor layers containing impurities of the memory cell satisfy the conditions as defined in claim 5~~ the plural semiconductor layers include a p-type third layer arranged to form an additional junction positioned shallower than the depth of the device isolation region.

14. (Currently Amended) A semiconductor memory device as defined in claim 3, wherein the conductive layer of the memory cell is ~~a conductive layer connected~~ to formed as part of a same conductive layer as a gate electrode of an ~~insulate~~ insulated gate field effect transistor in the peripheral circuit.

15. (Currently Amended) A semiconductor memory device as defined in claim 3, wherein the conductive layer of the memory cell comprises a multi-layer containing ~~N-type~~ n-type or ~~P-type~~ p-type ~~polycrystal~~ polycrystalline silicon.

16. (Currently Amended) A semiconductor memory device as defined in claim 3, wherein the insulating layer of the memory cell is an insulating layer connected with an insulating layer of an insulated gate field effect transistor in the peripheral circuit.

17. (Original) A semiconductor memory device as defined in claim 1, wherein the insulating layer of the memory cell is a multi-layer of insulating layers having different band gaps.

18. (Currently Amended) A semiconductor memory device as defined in claim 17, wherein the insulating layer of the memory cell comprises a multi-layer of a silicon oxide layer and a silicon nitride layer and the silicon oxide layer is ~~present~~ in contact with a ~~p-type~~ p-type semiconductor layer formed in a silicon substrate.

19. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein at least one of the plural semiconductor layers ~~containing the impurities of the memory cell is present~~ extending in a direction perpendicular to the word ~~line~~ lines in the semiconductor substrate.

20. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein ~~the layer in contact with the insulating layer for forming the memory cell among the plural semiconductor layers containing the impurities of the memory cell is present being separated on every~~ a respective one of the plural semiconductor layers in contact with the insulating layer in each

memory cell is separated from the corresponding semiconductor layer of the other memory cells.

21. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein a conductive plug is electrically connected to a layer formed in the a lowest portion among of the plural semiconductor layers ~~containing impurities of the memory cell~~.

22. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein a layer formed at the a lowest portion among of the plural semiconductor layers ~~containing impurities of the memory cell~~ is electrically connected with a conductive layer extending in direction perpendicular to the word lines in a planer arrangement.

23. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein a layer ~~present~~ extending in a direction perpendicular to the word ~~line~~ lines in the ~~planer~~ same plane ~~arrangement among~~ as the plural semiconductor layers ~~containing the impurities of the memory cell~~ is electrically connected with ~~one of~~ a

diffusion ~~layers~~ layer of ~~the~~ a first insulated gate field effect transistor formed in the semiconductor substrate and is connected electrically with the conductive layer ~~extending~~ that also extends in the direction perpendicular to the word ~~line~~ lines ~~in the planer arrangement for the other of the diffusion layers of the insulated gate field effect transistor.~~

24. (Currently Amended) A semiconductor memory device including plural memory arrays each comprising:

plural word lines;

plural data lines arranged so as to intersect the plural word lines in a planer arrangement;

plural memory cells which are disposed each at a desired intersection between the plural word lines and the plural data lines and each connected to the corresponding word line and corresponding data line;

a common data line disposed in common with the plural data lines; and

plural signal tranamission means having a switching function for connecting the common data line to the plural data lines respectively;

wherein the ~~each~~ memory cell has a multi-layer of a conductive layer, an insulating layer and [[a]] plural semiconductor layers containing impurities, and a potential ~~can be~~ applied to the insulating layer that enables movement of the carriers by way of the multi-layer, and at least said plural semiconductor layers are disposed below a surface of a semiconductor substrate.

25. (Currently Amended) A semiconductor memory device including plural memory arrays each comprising:

plural word lines;

plural data lines arranged so as to intersect the plural word lines in a planer arrangement;

plural memory cells which are disposed each at a desired intersection between the plural word lines and the plural data lines and each connected to the corresponding word line and corresponding data line, a common data line disposed in common with the plural data lines; and

plural signal transmission means having a switching function for connecting the common data line to the plural data lines respectively;

wherein the memory cell has a multi-layer of a conductive layer, an insulating layer and [[a]] plural semiconductor layers containing impurities, and

the multi-layer of the memory cell has a bistable characteristic of a resistance value,

a potential applied to the insulating layer enables movement of carriers through the multi-layer, and

at least said plural semiconductor layers are disposed below a surface of a semiconductor substrate.

26. (Currently Amended) A semiconductor memory device including plural memory arrays each comprising:

plural word lines;

plural data lines arranged so as to intersect the plural word lines in a planer arrangement;

plural memory cells which are disposed each at a desired intersection between the plural word lines and the plural data lines and each connected to the corresponding word line and corresponding data line;

a common data line disposed in common with the plural data lines; and

plural signal transmission means having a switching function for connecting the common data line to the plural data lines respectively;

wherein ~~the~~ a memory cell has a multi-layer of a conductive layer, an insulating layer enabling a tunnel effect and [[a]] plural semiconductor layers containing impurities, ~~and~~ the plural semiconductor layers containing the impurities are ~~present in the~~ below a surface of a semiconductor substrate and a potential applied to the insulating layer enables movement of carriers through the multi-layer.

27. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein at least ~~the~~ each memory cell is formed on an On SOI substrate.

28. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein plural bit lines have one sense amplifier in common in ~~the~~ a memory cell array region.

29. (Cancelled)

30. (Currently Amended) A semiconductor memory device as defined in claim 1, wherein at least a portion of [[a]] the memory device is disposed in the semiconductor substrate and a memory capacity is 256 Mbits or more.

CLAIM 31 (CANCELLED)

a step of depositing an interlayer insulating layer, then opening a contact hole and burying a conductive body into the contact; and

a step of forming a bit line in the memory cell array region and a local interconnect layer in the peripheral circuit region.

32. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit disposed on the semiconductor substrate;

wherein ~~the~~ each memory cell has a multi-layer of a conductive layer, an insulating layer and plural semiconductor layers containing impurities, and

a current that flows when a potential is applied to the insulating layer is capable of moving carriers by way of the multi-layer and has a hysteresis characteristic relative to the applied voltage, and

at least said plural semiconductor layers are disposed below a surface of the semiconductor substrate.

33. (Currently Amended) A semiconductor memory device as defined in claim 5, wherein an impurity concentration of the a layer present in contact with the surface of the semiconductor substrate among of the plural semiconductor layers ~~containing impurities for forming the memory cell~~ is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.

34. (Currently Amended) A semiconductor memory device as defined in claim 6, wherein an impurity concentration of the a layer present in contact with the surface of the semiconductor substrate among of the plural semiconductor layers ~~containing impurities for forming the memory cell~~ is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.

35. (Currently Amended) A semiconductor memory device as defined in claim 7, wherein an impurity concentration of the a layer present in contact with the surface of the semiconductor substrate among of the plural semiconductor layers ~~containing impurities for forming the memory cell~~ is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.